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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/614,286	07/12/2000	Hiroshi Tanabe	NECK 17.552	2375

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EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/614,286	TANABE, HIROSHI	
	Examin r	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6-8 and 11-14* is/are pending in the application.

4a) Of the above claim(s) *11-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4 and 6-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7 January 2004 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "the first-property semiconductor film" in the last line. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites the limitation "the second-property semiconductor film" in the last line. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **1**, 4, 6, **7**, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the article **Im** et al. "Single-crystal Si films for thin-film transistor devices" Applied Physics Letters 70(25) 23 June 1997, pp. 3434-3436 (the article provided by Applicant) in view of US 6,136,632 (**Higashi**) and US 5,821,562 (**Makita** et al.).

Regarding claims 1, 4, 6, and 7, **Im** discloses a method for forming a crystalline (i.e. second property) semiconductor film at a desired position on a substrate comprising,

preparing a substrate having deposited thereon, amorphous (i.e. first property) semiconductor silicon (a-Si);

preparing an optical mask having a pattern thereon and spacing the mask apart from the substrate;

positioning the mask at the desired position;

irradiating the a-Si through the mask pattern to convert the desired exposed regions to polycrystalline and single crystalline (i.e. second property) semiconductor silicon, wherein the amorphous (non-irradiated) silicon has an optical property different from the single crystalline (irradiated) silicon as shown in Figs. 1 and 2, and wherein the crystallized silicon film is used for the production of thin film transistors TFTs.

(See whole article -- especially the Abstract, paragraph bridging the cols. on p. 3434 and p. 3436, left-hand col., last paragraph.)

Im does not indicate that the difference between the optical properties of the amorphous and crystalline silicon films, as shown in Figs. 1 and 2, are used as an alignment mark. However,

Im does state that "the number and location of these [crystallized silicon] regions can be precisely controlled by using an appropriately patterned mask." (Im p. 3435, left-hand col. last sentence of penultimate paragraph.) This indicates that **Im** suggests precisely controlling the location of each of the crystallized regions.

Higashi --like **Im**-- teaches the irradiation of amorphous silicon to form crystalline silicon which is then patterned to form crystalline semiconductor islands used to form TFTs. **Higashi** teaches that the optical property difference between the amorphous and crystalline silicon is used as an alignment for positioning a mask used to carry out the patterning to form islands for forming TFTs. In this regard Higashi states beginning at col. 10, line 4,

> "After the annealing process, the silicon film 30 is patterned using a photolithography technique so as to form islands 31 of the silicon film as shown in FIG. 4(C), FIG. 5(D), and FIG. 9. In this patterning process, the alignment between a mask pattern used in the patterning process and an annealing pattern generated by the laser annealing process performed on the silicon film 30 is performed using the color of the silicon film 30 subjected to the laser annealing which varies depending on the degree of the irradiation of the laser beam LO. That is, **those regions of the silicon film 30 which are not irradiated by the laser beam LO and thus remain in the form of amorphous silicon are red, while those regions of the silicon film 30 which have been converted into the polycrystalline form by irradiation of the laser beam LO are yellow. The boundary between a red and yellow regions is used as a reference line by which the mask pattern for the above patterning is aligned relative to the annealing pattern of the silicon film 30.** If laser annealing is performed at spatial intervals corresponding to the pixel pitch PY in the Y direction, the mask alignment can be properly performed with respect to the annealing alignment pattern so that pixel TFTs with small variations can be formed with high throughput." (Emphasis added.)

If it were not already completely obvious to one of ordinary skill that the differences in optical properties between the amorphous and crystalline silicon films as shown in **Im** could be

used as an alignment mark, it would have been made obvious for one of ordinary skill in the art, at the time of the invention by the teaching in **Higashi** since **Higashi** specifically uses said differences in optical property as an alignment marks for further positioning of masks to carry out patterning for TFT fabrication. One of ordinary skill would be especially motivated to use the differences in optical property as an alignment mark because no additional steps are required to form the alignment mark resulting in a dramatic reduction in time and money used to fabricate the semiconductor devices, which is always highly desired in the semiconductor fabrication art to increase throughput without additional cost.

Then the only difference is that **Im** does not indicate that an insulation film is formed on both the crystalline silicon and a-Si (i.e. the first property semiconductor film and the second property semiconductor film). And regarding claim 8, **Im** also does not indicate that the silicon film is patterned to form crystalline silicon islands. However, **Im** does indicate that the crystallized silicon film --especially the single crystal region-- is used to form a TFT which suggests to one of ordinary skill that additional processing to form the TFT will be necessary.

Makita teaches a method of forming a TFT by blanket depositing an amorphous silicon film **402** (Fig. 10B), and then forming an insulation film **413** (Fig. 10J) over the both the first property and the second property silicon films **402**, and **412** to serve as a gate dielectric (Fig. 10K). (See Figs. 10A to 10O and associated text beginning at col. 22, line 30).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to blanket deposit the insulation film of **Makita** over both the a-Si and crystallized silicon of **Im** in order to form the gate dielectric of the TFTs and the alignment marks used to position the rest of the layer, as taught to be beneficial in **Makita**. The patterning to form islands is standard in

the art for TFT fabrication as shown in **Makita** and is an obvious modification to **Im** because **Im** teaches that the single crystal silicon region is the best for forming a TFT.

Double Patenting

6. Applicant is advised that should claim 6 be found allowable, claim7 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Response to Arguments

7. Applicant's arguments with respect to claims 1, 4, 6, 7, and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erik Kielin
Primary Examiner
11 May 2004